The Applicant's invention is directed to a method for forming a self-aligned contact. In the method, a conformal dielectric liner layer is formed on the substrate before the main dielectric layer is formed. Then, ***a self-aligned contact*** is formed through the dielectric layer and the liner layer to contact with the substrate. As shown in FIG. 2A~2D, the liner layer 204 is formed under the dielectric layer 206, and a self-aligned contact window 210/self-aligned contact 214 is formed through the dielectric layer 206 and the liner layer 204.

Discussion of Office Action Rejections

As mentioned above, the invention provides a method for forming a self-aligned contact, in which ***a self-aligned contact is formed*** through the dielectric layer and the liner layer. The feature of the method is recited with underlines in independent claims 1, 6 and 12 and the amended independent claim 15 as follows:

1. A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a dielectric liner layer over the semiconductor device;

forming a dielectric layer over the dielectric liner layer; and

patterning the dielectric layer and the dielectric liner layer without planarizing the dielectric layer, to form a self-aligned contact window that exposes a surface of the substrate between the said first and second gates.

6. A method of forming a contact plug in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a dielectric liner layer conformal to a surface profile of the substrate and the said first and second gates;

forming a dielectric layer over the dielectric liner layer;

patterning the dielectric layer and the dielectric liner layer without planarizing the dielectric layer, to form a self-aligned contact window that exposes a surface of the substrate between said first and second gates;

forming a polysilicon layer over the dielectric layer and filling the self-aligned contact window;

removing a portion of the polysilicon layer lying above the dielectric layer; and

removing a portion of the dielectric layer so that the contact plug is formed inside the self-aligned contact window.

12. A method of forming a contact plug in a semiconductor device comprising at least a first gate and a second gate over a substrate, wherein the said first and second gates have sidewall spacers, the method comprising the steps of:

forming a silicon nitride dielectric liner layer conformal to a surface profile of the substrate and the said first and second gates;

forming a silicon oxide dielectric layer over the substrate;

patterning the silicon oxide layer and the silicon nitride layer without planarizing the silicon oxide dielectric liner layer, to form a self-aligned contact window that exposes a surface of the substrate between the said first and second gates;

forming a polysilicon layer over the dielectric layer and filling the self-aligned contact window;

performing chemical-mechanical polishing to remove a portion of the polysilicon layer lying above the silicon oxide layer and a portion of the silicon oxide layer so that the landed plug is formed inside the self-aligned contact window.

15. A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate, with sidewall spacers, over a substrate, and a thin liner oxide layer disposed conformal to the surface profile of the substrate and the said first and second gates, the method comprising the steps of:

forming a dielectric layer over the semiconductor device; and

patterning the dielectric layer without planarizing the dielectric layer, to form a self-aligned contact window between the said first and second gates.

According to the Examiner's opinions, Yoon discloses forming a self-aligned contact window 106 in the dielectric layer 104 (FIG. 2B) and Jeong discloses forming a liner layer 77 before the insulating layer 81 for contact formation is formed (FIG. 4A~4D), and independent claims 1, 6, 12 and 15 of this invention therefore can be obtained by combining Yoon and Jeong. However, Applicant respectively disagrees based on the following reasons.

Yoon et al. provide a method for forming contact plugs, wherein a dielectric layer 104 is formed on the substrate 100, contact windows 106 are formed in the dielectric layer 104, and then contact plugs 108 are formed in the contact windows 106. Examiner states that contact windows

106 are self-aligned contact windows, ***however***, the contact windows 106 are actually ***not self-aligned contact windows*** because each of them is narrower than the substrate between two gate structures 102. In other words, a real self-aligned contact window ***should be wider than the substrate between two gate structures***, so as to have a self-alignment effect, i.e., to fully expose the substrate between two gate structures even with misalignments of the photolithography process. Therefore, Yoon ***fails to disclose forming self-aligned contact windows*** through the dielectric layer 104.

On the other hand, Jeong disclose a method for forming contact plugs, wherein a liner layer 77 is formed on the substrate, a gap-filling insulating layer 79 is filled into the gaps created by the liner layer 77, another insulating layer 81 is formed on 77 and 79, and then the insulating layer 81 and the liner layer 77 is etched to form via holes 82, as shown in FIG. 4A~4D. Since no self-alignment mechanism is used in the method, Jeong also ***fails to disclose forming self-aligned contact windows*** through the insulating layer 81 and the liner layer 77.

In summary, ***a self-aligned contact window is formed*** in each of independent claims 1, 6 and 12 and the amended independent claim 15, while Yoon et al. and Jeong ***both fail to disclose forming self-aligned contact windows***. Therefore, neither of independent claims 1, 6 and 12 and the amended independent claim 15 can be obtained by combining Yoon et al. and Jeong.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 6 and 12 and the amended independent claim 15 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 2~5, 7~11, 13~14 and 16~19 also define over the prior art even though their contents are disclosed more or less in the prior art references.

CONCLUSION

For at least the foregoing reasons, it is believed that all pending claims 1~19 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW WHERE CHANGES MADE

In The Claims

Please amend claim 15 as follows:

15. A method of forming a contact opening in a semiconductor device comprising at least a first gate and a second gate, with sidewall spacers, over a substrate, and a thin liner oxide layer disposed conformal to the surface profile of the substrate and the said first and second gates, the method comprising the steps of:

forming a dielectric layer over the semiconductor device; and

patterning the dielectric layer without planarizing the dielectric layer, to form a self-aligned contact window between the said first and second gates.